REMARKS

Claims 1-35 are pending. Claims 1-35 were rejected. In the previous office action, claims 1-32 were rejected under 35 U.S.C. 102(e) as being anticipated by Edirisooriya (2003/0195939A1), hereinafter Edi. Claims 33-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Edi. The Examiner has withdrawn the finality of the previous office action. The Applicants gratefully acknowledge the withdrawal of the finality of the previous office action. In the current office action, the Examiner has revised the rejections to claims 1-35 and is rejecting claims 1-35 under 35 U.S.C. 103(a) as being unpatentable over Edi in view of Iwasa (USP 5,241,641).

Edi describes a multiprocessor system that "includes a plurality of processors 12 and 14 that are communicatively coupled via an interconnection network 16. The processors 12 and 14 are implemented using any desired processing unit ... The interconnection network 16 is implemented using any suitable shared bus or other communication network or interface that permits multiple processors to communicate with each other and, if desired, with other system agents such as, for example, memory controllers ... Additionally, the processors 12 and 14 respectively include caches 22 and 24, cache controllers 26 and 28 and request queues 30 and 32." (Paragraphs 12-14) Edi also describes use of the MSI, MESI and MOESI protocols "to eliminate unnecessary data transfers between processors." (Paragraph 33) Edi does not mention multiple processor clusters and only describes multiple processors connected over an interconnection network such as a shared bus.

Iwasa describes a computer system. "The PROCESSOR block 80 (as shown in FIGS. 3A and 3B), in general, includes at least a microprocessor 81, and possibly a co-processor 82 and/or cache controller 83, which components are installed at the option of the end user for enhanced performance. Although the type of components (i.e., the microprocessor 81, co-processor 82, and cache controller 83) in the PROCESSOR block 80 are not limited to those shown in FIGS. 3C to 3F, they must be compatible with the 80X86 Intel family of microprocessors. In other words, the components must be PC compatible." (Column 5, lines 13-24)

The Examiner argues that Edi states "persons of ordinary skill in the art will recognize that the multiprocessor system 10 may include additional processors or agents that are also communicatively coupled via the interconnection network 16, if desired." (Paragraph 18) Edi

mentions that "while the interconnection network 16 is preferably implemented using a hardwired communication medium, other communication media, including wireless media, could be used instead." (Paragraph 13) The only example of an interconnection network Edi provides is a "shared bus." (Paragraphs 3 and 13)

Having multiple processors connected over an interconnection network does not teach or suggest clusters of processors. The independent claims 1, 16, 26 and 33 all recite a "home cluster" including a "plurality of processing nodes" and a "remote cluster" including a "plurality of processing nodes." A home cluster and a remote cluster are described throughout the present application and examples are depicted throughout in the Figures, e.g. Figures 1A, 1B, 2, 11, and 12 and associated description. Edi does not teach or suggest any home cluster or remote cluster. Furthermore, Edi does not teach or suggest any home cluster including a plurality of processing nodes or any remote cluster including a plurality of processing nodes. The Examiner argues that a remote cluster is "other processing nodes 14" shown in Figure 1 of Edi. The Applicants respectfully disagree. Edi merely depicts a conventional architecture in Figure 1 and associated description with a processor 12 connected to a processor 14 over a shared bus 16. No clusters are shown. No clusters of processing nodes are shown. Even if we were to hypothetically add numerous additional processors to the Edi system, nothing in Edi teaches or suggests separating the processors into processor clusters. The flows charts in Figures 2 and 3 and the associated description merely depict interactions between multiple processors connected over a bus 16. Figures 4a-4d and associated description also similarly only show "various states through which the multiprocessor system 10 shown in FIG. 1 progresses." No clusters are depicted, taught, or even suggested.

The Examiner also argues that Edi may not sufficiently teach or suggest clusters of processors including a home cluster and remote clusters with the "first plurality of processing nodes and the home cache coherence controller interconnected in a point-to-point architecture." The Examiner argues that Iwasa describes this element. The Examiner argues that Figure 1 and Figure 3 along with column 3 lines 66 et seq teach or suggest processors and a cache controller interconnected in a point-to-point architecture.

The Applicants respectfully disagree. Figure 1 and 3 themselves are somewhat ambiguous as to how processors and a cache coherence controller are connected. The description however, provides some clarification. The description in no way teaches or suggests

multiple processors and a cache coherence controller interconnected in a point-to-point architecture. Instead, the description makes ample reference to the use of a shared bus. A conventional shared bus architecture is not a point-to-point architecture. "As an example, FIG. 3C shows a block diagram of the PROCESSOR block 80 including a 80386-type microprocessor 81a, 80387-type co-processor 82a, and 82396-type cache controller 83a coupled to the local bus 40. The interconnection of these components to the processor bus 84 is conventional and well within the skill of those familiar with this art." (column 5, lines 25-30)

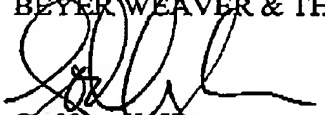
Furthermore, Iwasa emphasizes that the shared bus and processor architecture used must be compatible with a conventional Intel processor system. Iwasa indeed uses the word "must." Although the type of components (i.e., the microprocessor 81, co-processor 82, and cache controller 83) in the PROCESSOR block 80 are not limited to those shown in FIGS. 3C to 3F, they must be compatible with the 80X86 Intel family of microprocessors. In other words, the components must be PC compatible." (Column 5, lines 17-24) Processors in the 80X86 Intel family or microprocessors do not support multiple processors and a cache coherence controller interconnected in a point-to-point architecture.

In addition, claim 1 includes the recitation "identify a processing node from the second plurality of processing nodes that owns a cache line corresponding to the probe, and send a targeted probe to the processing node" and claims 16, 26, and 33 recite "identifying owning node information... [and] maintaining owning node information associated with the home cluster." The Examiner argues that Edi describes determining whether the cache block associated with a request is in an owned state. However, Edi does not teach or suggest identifying the processing node that owns the cache line. Conventional systems such as Edi only provides MEOSI state information for a particular cache line and do not identify the node or processing node owning the cache line.

The techniques of the present invention recognize that this is beneficial for a variety of reasons. For example, "a coherence directory is used to eliminate the transmission of a request to a memory controller in a home cluster. A coherence directory can also be used to more accurately send targeted probes. In one example, only a node owning a particular memory line needs to be probed. Information can be added to probe requests and probes to identify the owning node and allow probes to be directed only at owning nodes in a given cluster." (page 9, lines 1-6)

Consequently, the rejections to independent claims 1, 16, 26, and 33 are believed overcome. In light of the above remarks relating to independent claims the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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